

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 08/903,453

Filing Date: July 29, 1997

Title: CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

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67. [New] The memory cell of claim 52 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.
68. [New] A transistor comprising:
a source region in a substrate;
a drain region in the substrate;
a channel region between the source region and the drain region in the substrate;
a floating gate; and
means for separating the floating gate from the channel region.

REMARKS

In response to the Office Action dated 24 October 2000, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-6 and 20-64 are pending in the application, and are rejected. Claims 1-5, 20, 21, 24, 29, 31, 32, 35, 36, 38-48, and 50-64 have been amended, and new claims 65-68 have been added. No new matter has been added.

Double Patenting

The Examiner provisionally rejected claims 1-6 under the judicially created doctrine of obviousness-type double patenting over claims 11-18 of copending Application Serial No. 08/902,843. The applicant respectfully submits that the amendments made herein to claims 1-5 have rendered these claims even more patentably distinct from the claims in Application Serial No. 08/902,843. The applicant respectfully requests that this provisional rejection be withdrawn.

Rejection of Claims under 35 USC § 102(b)

Claims 4, 5, 20, 23, 29, 32, and 36 were rejected under 35 USC § 102(b) as being anticipated by Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata). The applicant respectfully traverses.

Claim 20 recites a memory cell comprising a floating gate and a layer of amorphous carburized silicon grown on a substrate and located between the floating gate and the substrate.

Sakata does not disclose a layer of amorphous carburized silicon grown on a substrate as recited in claim 20. Sakata discloses in Figure 1 a diode structure comprising c-Si, a film of hydrogenated amorphous silicon carbide (a-SiC:H), a film of hydrogenated amorphous silicon (a-Si:H), another film of a-SiC:H, and Al. Column 3. Both the a-SiC:H and the a-Si:H films are deposited according to the process described in column 2 of Sakata under the heading "Sample preparation."

The applicant respectfully submits that Sakata does not disclose the layer of amorphous carburized silicon grown on a substrate as recited in claim 20, that claim 20 is not anticipated by Sakata, and that claim 20 is in condition for allowance.

Claims 4, 5, 23, 29, 32, and 36 recite limitations similar to those recited in claim 20. For reasons analogous to those stated above with respect to claim 20, and the limitations in the claims, that applicant respectfully submits that claims 4, 5, 23, 29, 32, and 36 are not anticipated by Sakata, and that these claims are in condition for allowance.

Rejection of Claims under 35 USC § 103(a)

Claims 1-3, 6, 21, 22, 24-30, 33-34, 37, 39, 41, 44-46, and 50 were rejected under 35 USC § 103(a) as being unpatentable over Sakata. The applicant respectfully traverses.

Claim 1 recites an integrated circuit field effect transistor comprising an amorphous carburized silicon layer gate insulator that was grown on a substrate.

For reasons analogous to those stated above with respect to claim 20, the applicant respectfully submits that Sakata does not disclose an amorphous carburized silicon layer gate insulator that was grown on a substrate as is recited in claim 1. The Examiner argued that the addition of a source, a drain, a channel, and a semiconductor surface layer on an underlying insulating portion to the disclosure of Sakata would have been obvious to one skilled in the art. However, the Examiner has not shown a teaching or motivation to combine these additional elements with Sakata, as is required by *In re Dembiczak*, 50 USPQ2d 1614 (Fed. Cir. 1999). In addition, the Examiner's suggestions do not supply another element recited in claim 1 that is

missing in Sakata, the amorphous carburized silicon layer gate insulator that was grown on a substrate.

The applicant respectfully submits that Sakata does not disclose or suggest all of the elements recited in claim 1, and that claim 1 is in condition for allowance. Claims 2-3, 6, 21, 22, 24-30, 33-34, 37, 39, 41, 44-46, and 50 recite limitations similar to those recited in claim 1. For reasons analogous to those stated above with respect to claim 1, and the limitations in the claims, that applicant respectfully submits that claims 2-3, 6, 21, 22, 24-30, 33-34, 37, 39, 41, 44-46, and 50 are not anticipated by Sakata, and that these claims are in condition for allowance.

Claims 31, 35, 38, 40, 42, 43, 47-49 and 51-64 were rejected under 35 USC § 103(a) as being unpatentable over Sakata in view of Sugita (JP Patent No. 08-255878). The applicant respectfully traverses.

Claim 48 recites a transistor comprising, among other elements, a floating gate separated from a channel region by a layer of amorphous carburized silicon that was grown on a substrate.

For reasons analogous to those stated above with respect to claim 20, the applicant respectfully submits that Sakata does not disclose a layer of amorphous carburized silicon that was grown on a substrate as is recited in claim 48.

The Examiner suggested that it would have been obvious to add the polysilicon gate disclosed in Sugita to the device of Sakata. The Examiner stated that these references were combinable because they were from the same field of endeavor. However, this is contrary to the law as stated in *In re Dembiczak*, which requires a showing of a clear and particular teaching or motivation to combine Sugita and Sakata. 50 USPQ2d at 1614. Such a general allegation is not sufficient.

Furthermore, the disclosure in Sugita of a polysilicon gate does not supply the element missing in Sakata, the layer of amorphous carburized silicon that was grown on a substrate as recited in claim 48.

The applicant respectfully submits that the combination of Sakata and Sugita does not disclose or suggest all of the elements recited in claim 48, and that claim 48 is in condition for allowance. Claims 31, 35, 38, 40, 42, 43, 47, 49 and 51-64 recite limitations similar to those recited in claim 48. For reasons analogous to those stated above with respect to claim 48, and the

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limitations in the claims, that applicant respectfully submits that claims 31, 35, 38, 40, 42, 43, 47, 49 and 51-64 are not disclosed or suggested by the combination of Sakata and Sugita, and that these claims are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date 23 February 2001

By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23 day of February, 2001.

Name

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